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AHB INTERFACE WITH SPI MASTER BY USING VERILOG

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ABSTRACT

In this paper the power consumption of AHB SPI-Master is being optimized by using RTL clock gating technique. SPI (Serial Peripheral Interface) is a serial interface which facilitates the synchronous serial data transfer between 2 devices. It operates in master and slave modes. AMBA (Advanced Microcontroller Bus Architecture) is an on chip bus developed by ARM Ltd. and is widely used in Soc designs. AHB (Advanced High Performance Bus) is a high frequency and high bandwidth bus which comes under AMBA classification. The AMBA-AHB slave interface programs the SPI registers. The RTL clock gating technique is used for reducing dynamic power consumption. The overall design comprises of AHB- slave interface, SPI-master, SCLK generator, gated clock and memory. RTL coding is done in verilog. Simulations are observed in MODELSIM simulator and power is calculated by loading the design in Lattice diamond FPGA kit. Power comparison is done by taking 50 MHzfrequency.

Keywords *– SPI (Serial Peripheral Interface), MOSI (Master Out Slave In), MISO (Master In Slave Out), SCLK (SPI Clock), SS (Slave Select) AMBA (Advanced Microcontroller Bus Architecture), AHB (Advanced High Performance Bus), RTL (Register Transfer Level), FPGA (Field Programmable Gate array).*

INTRODUCTION

Data can be transferred by two ways either parallel or serial. Serial data transfer is quite advantageous as compared to parallel data transfer because of simple wiring and less interaction between the conductors of serial cables. SPI and I2C are two common examples of serial datatransfers.

SPI (Serial Peripheral Interface) is basically a four wire interface which is used for serial data transmission between two devices. It was created by Motorola and also known as Microwire. It can be operated as master or slave. For communication with other devices it uses four signals namely MISO, MOSI, SCLK and SS. MOSI and MISO are two signals on which data is transferred in and out from SPI. When operated as master, SCLK signal is generated by the master and SS signal is pulled low to select the slave for datatransfer.

AMBA was introduced by ARM Ltd. in 1996. It is widely used as on chip bus in SoC (System on Chip) designs. There are three buses defined within AMBA specification. AHB(Advanced High Performance Bus), ASB (Advanced System Bus) and APB (Advanced Peripheral Bus). The AMBA AHB is a high performance and high frequency bus which supports up to 16 masters, burst operation, split transactions and pipelining. Whereas, ASB is the first generation of AMBA system bus which also supports burst operations. For low power and slow peripherals APB is used, which is a low frequency bus and does not support pipelining and burst operation as compared to the above two buses.

RTL CLOCK GATING

In the traditional synchronous design style, used for most of the HDL and synthesis based designs, the system clock is connected to clock pin on every flip-flop in design. This results in three major components of power consumption .

- Power consumed by combinatorial logic whose values are changing on each clockedge.
- Power consumed byflip-flops.
- Power consumed by the clock buffer tree in thedesign.

The RTL Clock Gating technique had a potential of reducing both power consumed by flip flop and clock distribution network, whereas, the first component of power is smallest contributor to total power consumption. Dynamic power can contribute up to 50% of total power and RTL Clock Gating technique is the most common technique for reducing dynamic power. There are different RTL Clock Gating techniques available to thedesigners.

RTL Clock Gating can be grouped into three categories:

- Combinational RTL ClockGating
- System level RTL ClockGating
- Sequential RTL ClockGating

The Combinational RTL Clock Gating is a straight forward substitution to the RTL code. It reduces power by disabling the clock on registers when the output is not changing. The System-level RTL Clock Gating technique stops the clock for an entire design, effectively disabling all functionality. On the contrary, combinational and sequential selectively suspend clocking while the design continues to produce an output. The Sequential RTL Clock Gating alters the RTL micro-architecture without affecting design functionality. Sequential clock-gating is a multi-cycle optimization with multiple implementation tradeoffs and RTL modifications.

BLOCK DIAGRAM

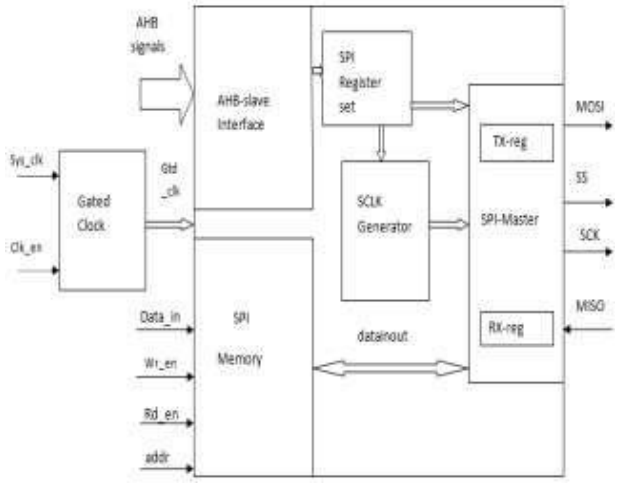

Fig. 1.AHB-Slave SPI-Master interface diagram with gated clock.

In fig.4.1, the system clock is gated by the gated clock block, when the clock enable (Clk_en) goes high, the clock will become active else it remains inactive. The gated clock is provided to the overall design. Here the AHB-slave interface is used for programming the SPI registers i.e. control register and SPI baud rate register. A memory is used for storing the data from SPI and providing the data to the SPI. When write enable (Wr_en) goes high data enters into memory through Data_in pin and when read enable (Rd_en) goes high data exits through data-inout pin to the SPI. This pin behaves like an in-out

pin. Then data enters into SPI TX-register at the gated clock which is provided to the whole module. Then, through SCLK generator block SCLK is generated for the master so that the data from the TX-register leaves SPI through MOSI on this SCLK and enters through MISO into RX-register on this SCLK. Now, the data in the RX-register will arrive on the data-inout pin which is an in-out port and enters into memory when the write enable goes high. Hence both transmitting and receiving the data is done.

FIGURES AND TABLES

Fig.2. Power calculation of without gated clock module at 50 MHz clock .

The total dynamic power consumed by the AHB-SPI interface is 12.4 mW and the static power is 94.5 mW at 50MHz system clock (non-gated clock) at 25 ˚C temperature.

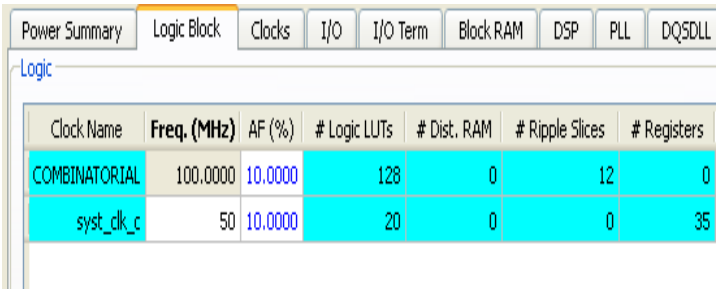

Fig.3.The number of LUTS and registers used by the design on the FPGA after place and route

Fig.4.Power calculation of with gated clock module at 50 MHz clock.

The total dynamic power consumed by the AHB-SPI interface is 4.9 m W and the static power is 92.1 mW at 50MHz gated clock at 25 ˚C temperature.

Fig.5. Number of LUTs and registers used by the design on FPGA after place and route.

The table shows the comparison of Dynamic power , LUTs used and registers used by both the designs**.**

Sr. no.	Factors	Non Gated clock	Gated clock
1.	Dynamic Power (mW)	12.4	4.9
2.	Number of LUTs used	148	145
3.	Number of registers used	35	35

Table 1. Comparison for 50 MHz clock

CONCLUSION

The comparison shows that the dynamic power consumed by the gated clock design is low as compared to non gated clock design. A difference of 7.5 mW is being observed between the gated clock and non gated clock architectures at 50MHz frequency and a difference of 7.4 mWat

75MHz frequency. Also the number of LUTs used by the gated clock is less as compared to the non gated clock architecture. The gated clock architecture uses 145 LUTs as compared to the non gated clock architecture which uses 148 LUTs. A difference of 3 LUTs is being observed. Hence, overall dynamic power is reduced by the RTL clock gatingtechnique.

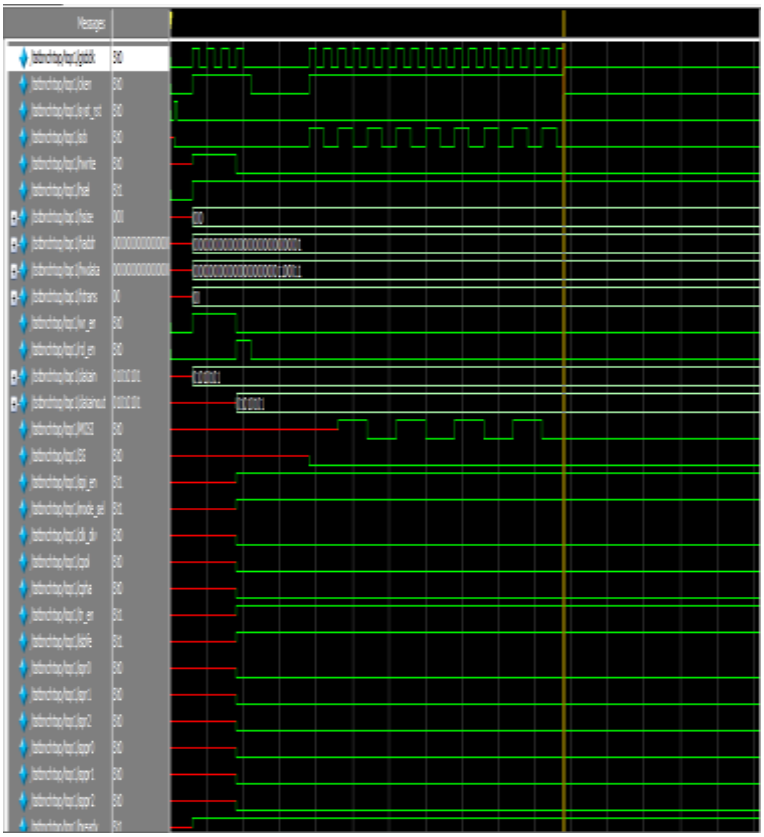

Fig 6: Output waveforms by Icarus simulating tool

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